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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/746,854	12/22/2000	James Morrow	10407/476	7292

7590 04/07/2004

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[REDACTED] EXAMINER

PATEL, NIKETA I

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 04/07/2004

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Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)
	09/746,854	MORROW ET AL.
	Examiner	Art Unit
	Niketa I. Patel	2182

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 23 January 2004.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-34 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-34 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 30 April 2001 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Specification

1. As indicated in the office action mailed on 08/19/2003, the title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-34 are rejected under 35 U.S.C. 102(e) as being anticipated by Laity et al. U.S. Patent Number: 6,697,892 (hereinafter referred to as "**Laity**".)

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4. **Referring to claims 1 and 19,** *Laity* teaches a generic device controller unit system for facilitating interaction between a processor and any number of peripheral devices, the system comprising [see Abstract]: a general purpose device controller [see figure 1 - elements 14,17,18,19,20,21,16; figure 2 - element 60] employing true real time peripheral device control [see figure 1 - element 52 'telephone line', 20 'RJ11'], wherein the device controller interfaces between a non-true real time operating system [see figure 1 - element 12; column 4 - lines 53-67; column 5 - lines 1-15] and the peripheral devices [see column 5 - lines 2-15, 35-59], thereby allowing a non-true real time operating system to implement true real time control of the peripheral devices [see column 1 - lines 66-67; column 2 - lines 1-37]; and a data and protocol communications interface, wherein the communications interface connects the processor and the peripheral devices, thereby allowing the processor to utilize a single protocol and associated data to communicate with the peripheral devices which may be utilizing protocols and associated data which are different than that used by the processor [see column 2 - lines 38-58.]

5. **Referring to claim 12,** *Laity* teaches a generic device controller unit [see figure 1 - elements 14,17,18,19,20,21,16; figure 2 - element 60] system for facilitating interaction .

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between a processor [see figure 1 - element 12] and any number of peripheral devices [see figure 1 - elements 52 'telephone line', 20 'RJ11', 44, 46, 40], the system comprising a general purpose device controller employing true real time peripheral device control [see figure 1 - elements 14,17,18,19,20,21,16; figure 2 - element 60]: wherein the device controller allows a non-true real time operating system to interface with various non-specific peripheral devices, thereby allowing a non-true real time operating system to implement true real time control of peripheral devices without a processor requiring either a real time kernel or a layered true real time operating system [see column 1 - lines 66-67; column 2 - lines 1-37; column 4 - lines 53-67; column 5 - lines 1-15.]

6. **Referring to claim 24, Laity** teaches a method for providing a data and protocol communications interface to facilitate interaction between a processor [see figure 1 - element 12] and any number of peripheral devices [see figure 1 - elements 52 'telephone line', 20 'RJ11'], the method comprising: interfacing between a non-true real time operating system and various non-specific peripheral devices [see figure 1 - elements 14,17,18,19,20,21,16; figure 2 - element 60]; employing true real time peripheral device control through a generic device controller unit, wherein the device controller allows the

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processor to implement true real time control of the peripheral devices without the non-true real time operating system requiring either a real time kernel or a layered true real time operating system [see column 1 - lines 66-67; column 2 - lines 1-37; column 4 - lines 53-67; column 5 - lines 1-15]; and providing a protocol and associated data communications interface between the processor and the peripheral devices, thereby allowing the processor to utilize a single protocol and associated data to communicate with the peripheral devices which may utilize different protocols and associated data then that used by the processor [see column 1 - lines 66-67; column 2 - lines 1-37; column 4 - lines 53-67; column 5 - lines 1-15.]

7. **Referring to claims 2, 13, 25, Laity** teaches that the generic device controller unit system produces true real time peripheral device control while interfaced with a non-true real time operating system running standard non-true real time software [see column 1 - lines 66-67; column 2 - lines 1-37; column 4 - lines 53-67; column 5 - lines 1-15.]

8. **Referring to claims 3, 14, 20, 26, Laity** teaches that the generic device controller unit system functions as a distributed processing environment [see column 1 - lines 66-67; column 2 - lines 1-37; column 4 - lines 53-67; column 5 - lines 1-15.]

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9. **Referring to claim 4, 27, Laity** teaches that the generic device controller unit system further includes customized system drivers [see column 1 - lines 66-67; column 2 - lines 1-37; column 4 - lines 53-67; column 5 - lines 1-15.]

10. **Referring to claims 5, 21, 28, Laity** teaches that Universal Serial Bus is the default communication protocol between the generic device controller unit system and the processor [see column 1 - lines 66-67; column 2 - lines 1-37; column 4 - lines 53-67; column 5 - lines 1-15.]

11. **Referring to claims 6, 18, 29, Laity** teaches that the generic device controller unit system interfaces with the non-true real time operating system that functions in a Win32 environment [see column 1 - lines 66-67; column 2 - lines 1-37; column 4 - lines 53-67; column 5 - lines 1-15.]

12. **Referring to claims 7, 15, 22, 30, Laity** teaches that the generic device controller unit system is an input/output device interface for a processor to peripheral devices [see column 1 - lines 66-67; column 2 - lines 1-37; column 4 - lines 53-67; column 5 - lines 1-15.]

13. **Referring to claims 8, 16, 31, Laity** teaches that the generic device controller unit system provides real time device control to resource management capabilities of a standard non-true real time operating system [see column 1 - lines 66-67;

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column 2 - lines 1-37; column 4 - lines 53-67; column 5 - lines 1-15.]

14. **Referring to claims 9, 17, 32, Laity** teaches that the generic controller unit system produces true real time peripheral device control without the higher level functionality of the processor [see column 1 - lines 66-67; column 2 - lines 1-37; column 4 - lines 53-67; column 5 - lines 1-15.]

15. **Referring to claims 10, 33, Laity** teaches that the generic device controller unit system produces true real time peripheral device control without the processor using a true real time kernel [see column 1 - lines 66-67; column 2 - lines 1-37; column 4 - lines 53-67; column 5 - lines 1-15.]

16. **Referring to claims 11, 34, Laity** teaches that the generic device controller unit system produces true real time peripheral device control without the processor utilizing a layered true real time operating system [see column 1 - lines 66-67; column 2 - lines 1-37; column 4 - lines 53-67; column 5 - lines 1-15.]

Response to Arguments

17. Applicant's arguments with respect to claims 1-34 have been considered but are moot in view of the new ground(s) of rejection.

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Conclusion

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following documents have been made record of to further show the state of the art as it pertains to real-time peripherals, which are controlled by a non-real time operating system:

- a. Molbak U.S. Patent Number: 6,494,776
- b. Harding et al. U.S. Patent Number: 6,524,230
- c. Korowitz et al. U.S. Patent Number: 6,671,763

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Niketa I. Patel whose telephone number is (703) 305 4893. The examiner can normally be reached on M-F 8:00 A.M. to 5:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A. Gaffin can be reached on (703) 308 3301. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NP
04/02/2003



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